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A system for trapping barium ions in a microfabricated surface trap

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We have developed a vacuum chamber and control system for rapid testing of microfabricated surface ion traps. Our system is modular in design and is based on an in-vacuum printed circuit board with integrated filters. We have used this system to successfully trap and cool barium ions and have achieved ion ‘dark’ lifetimes of $31.6 \text{ s} \pm 3.4 \text{ s}$ with controlled shuttling of ions. We provide a detailed description of the ion trap system including the in-vacuum materials used, control electronics and neutral atom source. We discuss the challenges presented in achieving a system which can work reliably over two years of operations in which the trap under test was changed at least 10 times. © 2014 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License. [<http://dx.doi.org/10.1063/1.4879817>]

Since the first demonstrated trapping of charged aluminum particles in a RF quadrupole trap in 1958^{1,2} the basic technology for trapping and cooling ions has become mainstream. The use of the electronic and motional states of trapped ions for storing quantum information was first proposed in 1995³ and initial demonstrations of the concept were achieved shortly thereafter.⁴ In the intervening years many key concepts of proposed quantum computer architectures^{5–8} have been demonstrated in trapped ions. These include very long coherence times,^{9–12} quantum logic gates,^{4,13–15} quantum algorithms¹⁶ and the entanglement of quantum states between multiple ions^{17–19} and between ions and photons.^{20–23} These demonstrations have typically been achieved at a small scale with just a few ions. However, a practical quantum computer with around 100 logical qubits would likely require coherent control of around 10^4 ions.²⁴ Contemporary ion trap technology requires a significant amount of space and support equipment for trap control, laser beam addressing, ion loading and maintaining vacuum. The technology is not practically scaleable. However, beyond some fundamental limits (for example, diffraction limited focusing of laser beams), technical scalability is generally considered to be an engineering.

One of the most promising designs for a technically scaleable ion trap is the microfabricated planar ion trap, first demonstrated in 2006.²⁵ Here, RF rails and DC bias electrodes are fabricated in an aluminum surface (sometimes gold coated) on silicon using semiconductor fabrication techniques.^{25,26} Such techniques are well known to be capable of high yield and mass manufacture. These traps are designed to trap an ion in a RF pseudopotential null $50 \text{ } \mu\text{m}$ to $200 \text{ } \mu\text{m}$ above the chip surface. A vapor of neutral atoms flows through an aperture in the back of the chip. Photo-ionization, laser cooling and optical pumping is done with beams passing just above the surface. After loading ions, the position of the trapping region can be finely controlled by adjusting the DC voltages on multiple electrodes on the trap surface while moving the lasers to follow the ions. Ultimately

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multiple trapping regions can be defined and ion chains can be re-organized by shuttling ions through junctions to different regions.

This concept allows very complex ‘chip traps’ to be mass-produced with features on the scale of 1×10^{-8} m. Chips with several designs of trapping regions have been produced. These include linear traps,^{27,28} multiple arm ‘Y’^{29,30} and ring traps.³¹ Novel features of recently fabricated chips include integrated optics for fluorescence light collection,^{32,33} integrated photodetectors,³⁴ integrated light sources³⁵ and integrated microwave waveguides.³⁶

Chip traps are currently fabricated by several groups around the world. We are working with devices provided by Sandia National Labs and Georgia Tech Research Institute (GTRI). Both these groups have standardized on a 100-pin architecture which gives the ability to control up to 96 DC electrodes. This standardization has allowed a high rate of trap development with at least 10 new chip designs developed in the past 3 years.

When compared with traditional macroscopic ion traps, the practical difficulties associated with the infrastructure required to control chip traps are significant. Reliable assembly by traditional methods of the number of systems likely required in a large scale ion-trap quantum computer is not practical. For this reason we have aimed to apply assembly and systems integration techniques common in the electronics industry to the rapid testing of new trap designs following the 100-pin standard.

Our particular interest is in $^{138}\text{Ba}^+$, an alkaline rare-earth metal isotope with nuclear spin-0. A key advantage of barium is that all important transitions for cooling and photo-ionization reside within either the visible or near-infrared spectrum, where coherent light sources are easily obtained and transmitted with optical fibers. This feature makes barium a good candidate for implementing a photonic link qubit as part of a large scale quantum computing architecture. Barium ions have been trapped in macroscopic traps of various designs since the 1980’s,^{37–40} though trapping of barium in a chip trap has not been demonstrated before.

I. CHAMBER DESIGN

Traditionally building an ion trap in a vacuum system involves wire wrapping and spot welding to make electrical connections. These techniques are well known to be compatible with the UHV environment and continued to be used once chip traps were developed. However, it was soon realized that these techniques do not scale well to chip traps which might require up to 100 connections to be made. Trap assembly is made tedious and error prone. Additionally, large numbers of point to point connections can reduce optical access and impede molecular flow.

In order to facilitate easy mounting and frequent upgrades we have designed a UHV-compatible printed circuit board (PCB) that holds a custom Zero-Insertion-Force (ZIF) socket⁴¹ for the chip trap. This socket accepts standard 100-pin ceramic Pin Grid Array (PGA) chip carriers used by GTRI and Sandia National Labs. These carriers are of a square design, 33.5 mm on each side with 0.5 mm pins arranged on the outside.

The circuit board plugs in to a set of four DB-25 female/female adapters⁴² which in turn are connected to feedthroughs integrated into the bottom flange⁴³ of the vacuum chamber. A grounding shield with a window of thin wire mesh clips on to the top of the chip carrier. The circuit board incorporates 20 nF 0805 series all-ceramic capacitors approximately 1 cm from the chip for filtering RF pickup on the DC control pins.

The circuit board is made of ceramic-filled Polytetrafluoroethylene (PTFE) material⁴⁴ of 1.52 mm thickness with a 35 μm copper cladding. It is a double sided board with plated through-holes. A particular difficulty with this material is its softness which causes it to be easily deformed by insertion pressure. In earlier iterations of the design without a ZIF socket these deformations lead to hairline cracks in the traces under the chip. We have found it important to minimize bending of the PCB during assembly and ensure all connections are tested prior to installing the chip. The PCB should have traces as wide as possible and maximize the available solder relief around pins.

Both the ZIF socket, DB-25 adapters and a small spacer on which the ZIF socket sits⁴⁵ are made of Polyether Ether Ketone (PEEK). The receptacle pins for holding the ZIF socket are a

gold plated brass alloy,⁴⁶ as are the pins which plug into the DB-25 connectors.⁴⁷ The pins for connecting the RF rails are longer⁴⁸ and pass through the circuit board without connection. They are then wire-wrapped⁴⁹ to a secondary feedthrough on the vacuum chamber. All on-board connections are soldered⁵⁰ and ultrasonically cleaned with flux remover⁵¹ followed by acetone before assembly.

The chamber is a ‘spherical octagon’ design.⁵² The chamber has eight 2.75 inch side ports, six of which provide optical access for the laser beams. Optical access for imaging occurs through a viewport on the top 6 inch port. Vertical space of approximately 25 mm is available underneath the circuit board for mounting the atomic vapor source. Figure 1 shows an exploded view of the trap chamber.

Pumping is done with an on-system 20 L/s ion pump and a titanium sublimation pump, each connected to a 2.75 inch 5-way junction on one of the chamber ports. After baking at 150 °C (as recommended by the chip manufacturer) for 1–2 weeks with a large ion pump and turbo-molecular pump we achieve a base pressure of a few 10^{-11} Torr. Exact final pressure and bake time depends on the number of new parts in the system and whether it was practical to back-fill with dry CO₂.

II. OPTICAL SETUP

An energy level diagram showing the relevant transitions for photo-ionization and doppler cooling of ¹³⁸Ba is shown in Figure 2.

The first step required in loading ions from an atomic vapor source is photo-ionization, either with a single UV source or combination of sources. Direct barium photo-ionization requires greater than 5.21 eV photon energy (238 nm). The accumulation of UV induced charges on trap components such as Macor[®] parts is a known problem with wavelengths below 500 nm and increases rapidly with shorter wavelengths.⁵³ The effect on PEEK and ceramic filled PTFE has not been characterized. In a chip trap surface charging is even more of a concern because the lasers must pass just 70 μm above the whole surface of the chip (around 1 cm path length). Therefore we require well focused beams with small divergence and wavelength as long as practical.

In barium, the traditional approach to photo-ionization has been to use a 791 nm laser to excite to the $6s6p\ ^3P_1$ state (1.57 eV), followed by a UV flash from a 337 nm nitrogen laser (3.68 eV) or UV flash lamp to complete the ionization.³⁹ An alternative approaches uses a 2-photon scheme with a single laser at 413 nm initially exciting the $5d6p\ ^3D_1$ and then ionizing.⁵⁴ Another recently demonstrated alternative uses a 553 nm laser to excite the strong dipole transition $6s^2\ ^1S_0 \rightarrow 6s6p\ ^1P_1$ followed by any laser with wavelength less than 418 nm to ionize.⁵⁵

To eliminate the use of far UV sources we use an ionization scheme in which we retain the traditional 791 nm laser and employ a secondary transition, $6s6p \rightarrow 6p^2$ (2.75 eV) driven with a 450 nm laser.⁵⁶ Finally, a tertiary transition is required, the 791 nm laser (or other cooling laser) can provide the necessary 0.91 eV to complete the ionization. An additional advantage of this scheme is improved isotope selectivity.

One difficulty encountered with this scheme is that after loading we observe immediate ‘shelving’ of the ion into the $D_{5/2}$ state. This process can be explained by a transition via the $7S_{1/2}$ level in the barium ion driven by incoherent light from the 450 nm laser. To solve this we require a third laser for de-shelving at 614 nm. This laser is obtained by frequency doubling a 1228 nm ECDL.⁵⁷ The addition of this laser is not an inconvenience because it can serve as a de-shelving laser for $D_{5/2}$ often needed in experiments.

Primary doppler cooling is done on the $S_{1/2} \rightarrow P_{1/2}$ transition at 493 nm. This beam is derived by frequency doubling⁵⁸ a 986 nm external cavity diode laser⁵⁹ (ECDL). This doubling arrangement is particularly advantageous because it allows fast switching via pickoff of a first order beam from an acousto-optic modulator (AOM) to be done in the IR. Optical aberrations and cross-talk in RF drive circuitry can reduce the isolation ratio achieved in a typical AOM switch setup. This has been a problem in earlier experiments. However due to the non-linearity of second-harmonic generation we achieve a very high isolation ratio which is not directly measurable. The lower limit to our isolation ratio measurement is 43 dB.

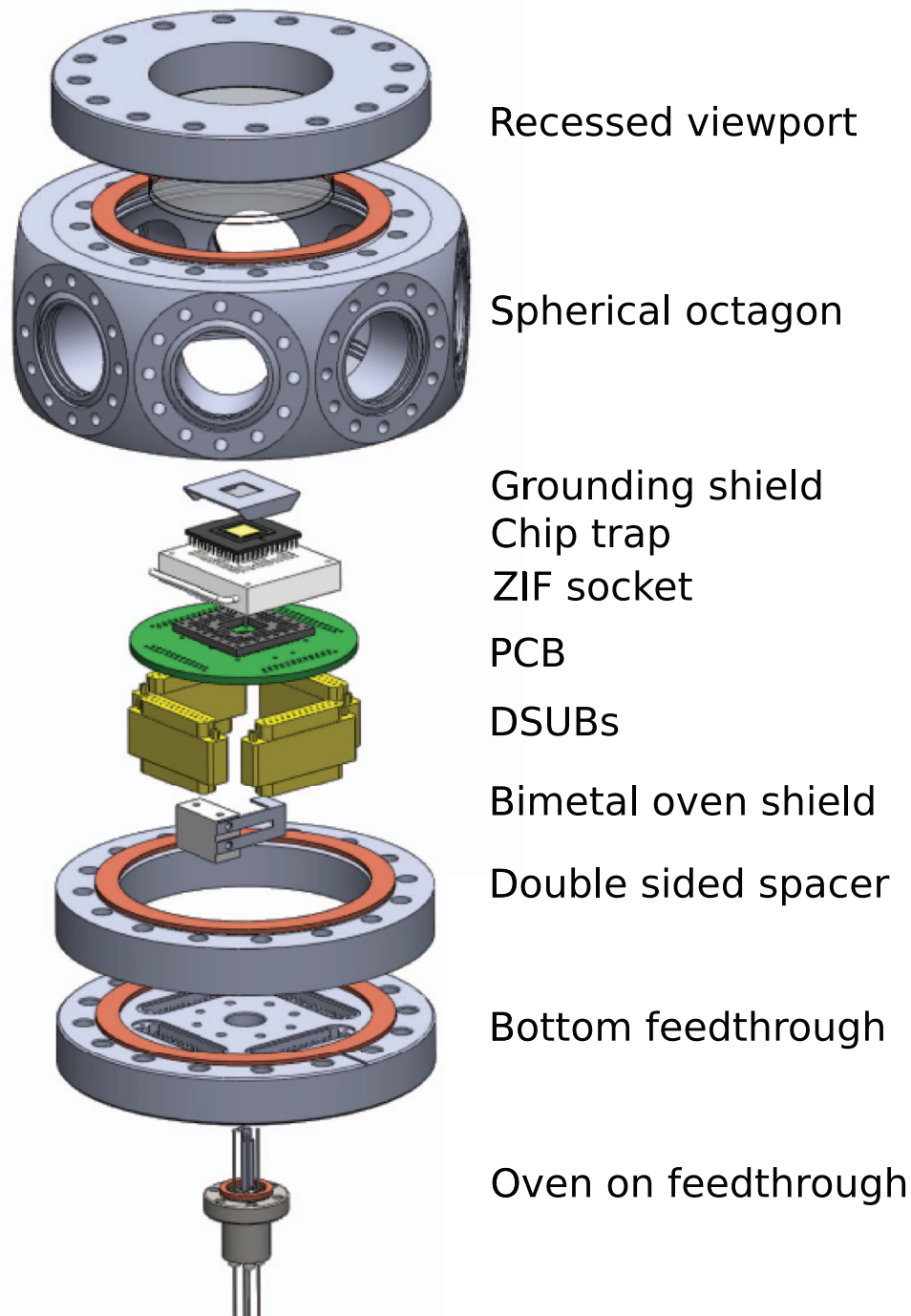


FIG. 1. Exploded view of trap chamber showing how the PCB, ZIF socket and chip trap are assembled in a spherical octagon UHV chamber.

A 650 nm laser is also required to re-pump out of the $D_{3/2}$ state. This is obtained from another ECDL.⁶⁰ Detecting the presence of poorly cooled ions in the initial stages of trapping is done by momentarily switching off this 650 nm laser and observing a decrease in 493 nm fluorescence signal.

Figure 3 shows a simplified representation of the optical setup for a single beamline. The 986 nm, 650 nm and 1228 nm lasers are each frequency locked to temperature stabilized invar

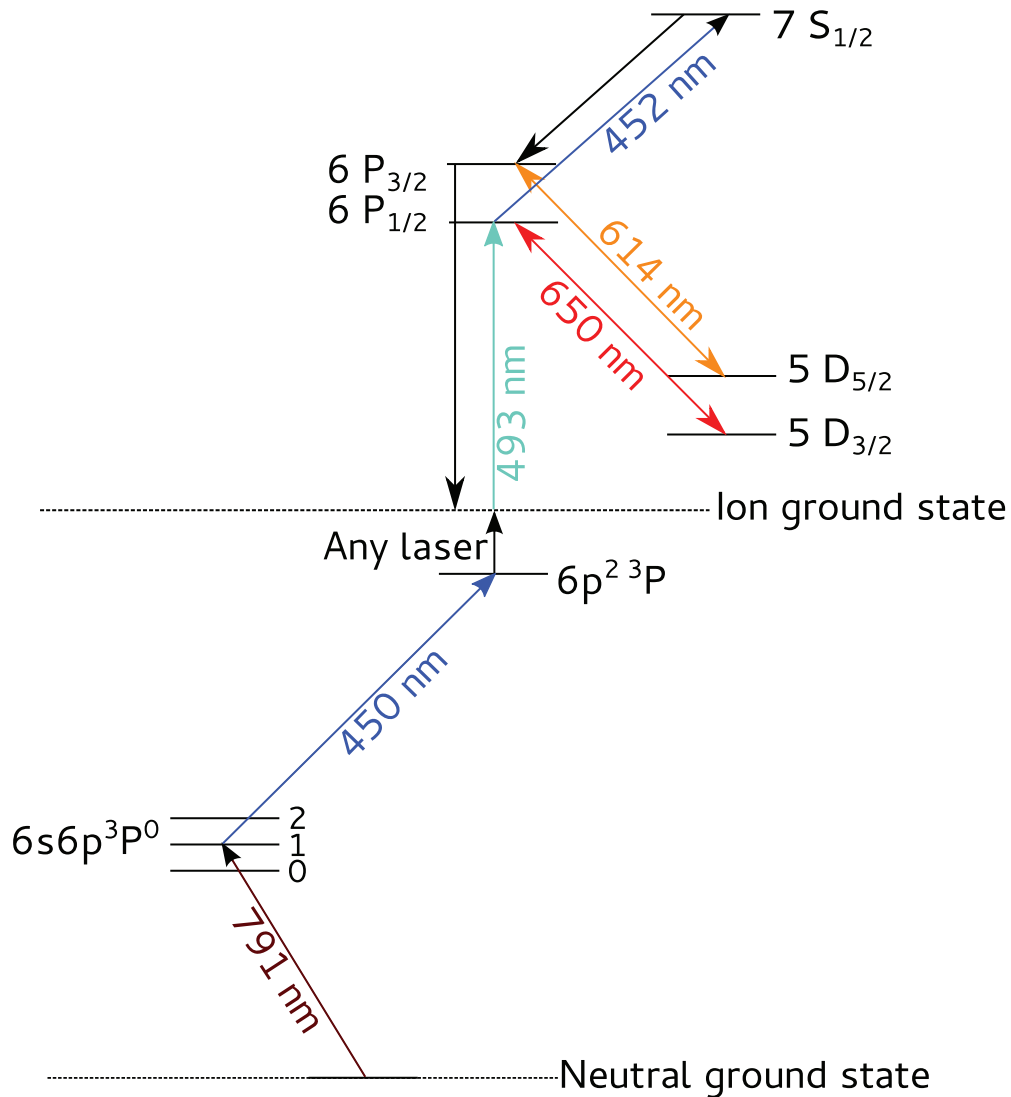


FIG. 2. Energy levels and laser transitions relevant for ionization and ion cooling in ^{138}Ba . Level information from Refs. 61 and 62. Approximate wavelengths of the laser driven transitions shown, for exact frequencies see Table I.

reference cavities in a hermetically sealed chamber using a custom top-of-the-fringe locking system. In each a zeroth-order beam from a switching AOM is passed through a double-passed AOM (DPAOM) setup to derive the beam to scan the cavity.

All of the beams except the 791 nm beam reside within the transmission spectrum of Nufern 460-HP optical fiber⁶³ and are coupled into a single optical fiber. This is particularly convenient for trapping operations because all four beams can be focused on the ion with a single setup. Coupling is achieved by first arranging combined ‘blue’ and ‘red’ beams from the 493 nm + 450 nm and 650 nm + 614 nm beams respectively each using polarizing beam splitters. These two combined beams are then further combined using a dichroic mirror⁶⁴ and coupled into the angle-cleaved end of an optical fiber.

The output of the fiber has a plane-cleaved end and an achromatic microscope objective is used to collimate the output beams. This is reflected by a piezo-controlled mirror⁶⁵ which allows the beam to be automatically pointed to the new ion position after shuttling. Finally a translatable lens is used for fine adjustment to focus the beams at the trapping region. Typical power levels for each of the beams at the fiber output and nominal trapping frequencies are shown in Table I.

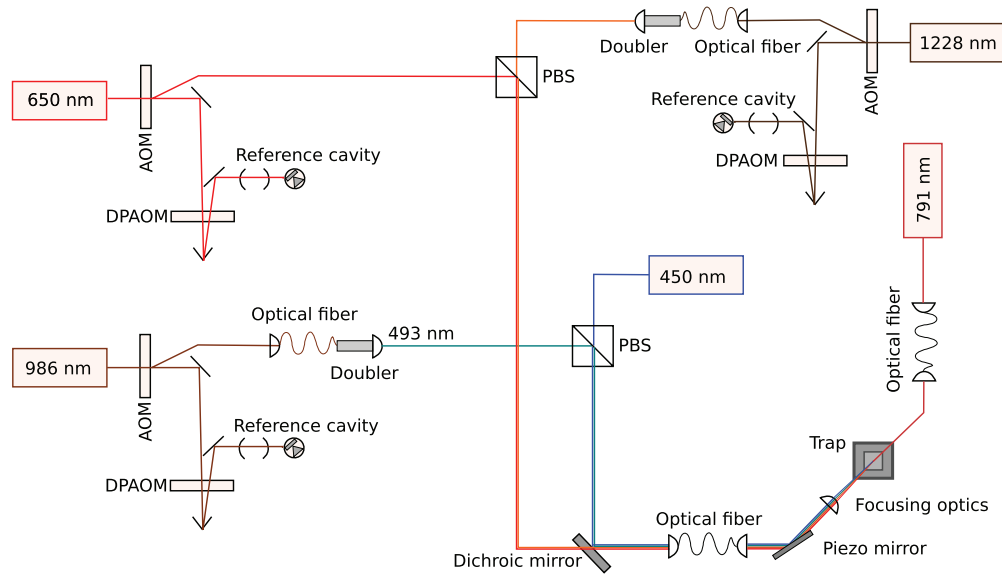


FIG. 3. Simplified schematic of the optical layout of the lasers required for ionization and laser cooling of barium. Note that the 4 visible lasers are coupled into a single optical fiber which greatly simplifies the delivery of light to the ion. Not shown are pickoffs for each of the beams to a wavelength meter which is used for tuning the exact laser frequencies.

TABLE I. Nominal laser operating frequencies and powers for photo-ionization and cooling.

Laser	Approx wavelength nm	Exact frequency THz	Power at ion μW	$1/e^2$ radius at ion μm
Primary ionization	791	378.83665	250	97
De-shelving	614	487.99008	0.5	76
Re-pump	650	461.31197	50	80
Secondary ionization	450	665.1433	250	55
Cooling	493	607.42659	5	61

Efficient collection of fluorescence light from the ion is important for robust state detection. Our chamber setup makes use of a custom top mounted recessed fused silica viewport which allows imaging optics to be placed within 20.7 mm of the trap surface. Otherwise our imaging system is conventional, employing a $20\times$ microscope objective⁶⁶ and second stage doublet lens.

The imaging beam path is split by a 50/50 beam splitter between a photomultiplier tube⁶⁷ (PMT) configured for photon counting and an electron-multiplying CCD camera.⁶⁸ A 493 nm optical bandpass filter can be switched in to the imaging beam path to block background light. Typical PMT count rates observed are 3000 counts/sec/ion against a background of 500 counts/s. Achieving a low background count rate requires tight focusing of beams and precise leveling relative to the chip surface.

The imaging stack is mounted on a translation stage which is actuated by NEMA-23 stepper motors coupled to the micrometers via a helical coupler and brass sliding square peg coupler. This allows the imaging system to be moved automatically to image ions in different locations on the trap surface.

III. VAPORIZATION

Obtaining a beam of neutral atoms presents some unique challenges when trapping barium in a chip trap.

1. Barium oxidizes readily in air and consequently the barium source must be protected from air during installation.

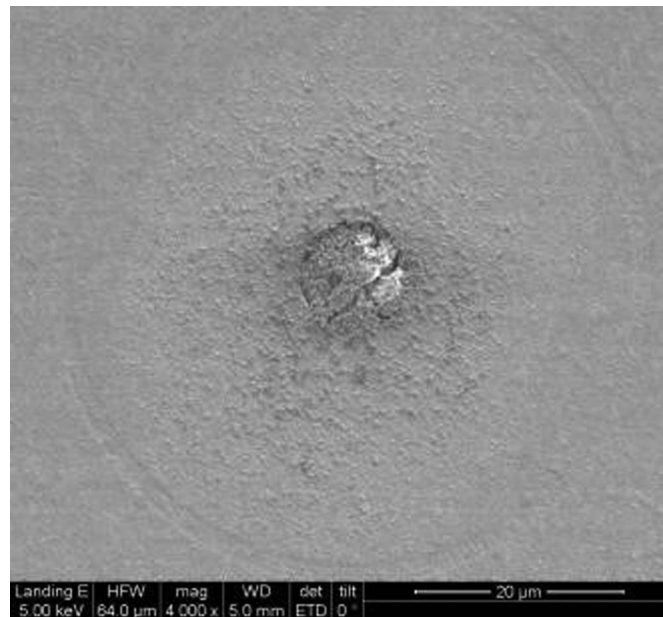


FIG. 4. SEM image of the surface of a Sandia ring trap post test with blocked loading hole. Figure courtesy of Sandia National Labs.

2. The fluorescence of neutral barium atoms at 791 nm is extremely weak and it has not been possible to use it to confirm the presence of neutral barium.
3. Blocking of the small loading apertures of chip traps with barium clusters can render a trap useless. Figure 4 shows a SEM image of the surface of a Sandia ring trap after testing with a traditional barium oven. This chip was also imaged with an energy-dispersive X-ray spectrograph (EDS) and the blockage identified as barium oxide.

The traditional approach to the oxidation problem has been to arrange an inert gas atmosphere and load fresh barium metal flakes into a thin alumina tube which is heated by a tungsten coil. Despite this precaution, some oxide is inevitably formed and the oven must initially run significantly hotter than usual to clean off the oxide layer. It is during this initial ‘break-in’ of a traditional oven that we expect the majority of the clusters seen in Figure 4 originate.

We have adopted a 2-part solution for reliable generation of neutral barium.

1. We use a commercial barium oven⁶⁹ in which the barium is contained in a stainless-steel tube filled with argon and sealed with indium. The indium seal breaks when the oven is heated. In operation the oven is heated by running current of up to 10 A through the tube. A small current (typically 5 A) is run through the oven during the bake-out of the chamber.
2. An oven shutter has been developed. This consists of a thermostatic bimetal strip⁷⁰ cut into an elongated ‘U’ shape with a stainless steel shutter attached. This is mounted to a Macor[®] block and mounted above the oven. When activated by running current through the strip it bends and moves the shutter to cover the oven tube. This protects the chip from excess barium flux and any indium from the seal. This is activated when the oven is run initially and continuously during chamber bake-out.

IV. ELECTRICAL SETUP

Because of the large number of DC electrodes which must be controlled, using off-the-shelf equipment quickly becomes cumbersome and expensive.

We have designed a custom electrode control system. It is based on three AD5372⁷¹ digital to analog converters (DACs) and controlled by a Cyclone II 2C35 field-programmable gate array

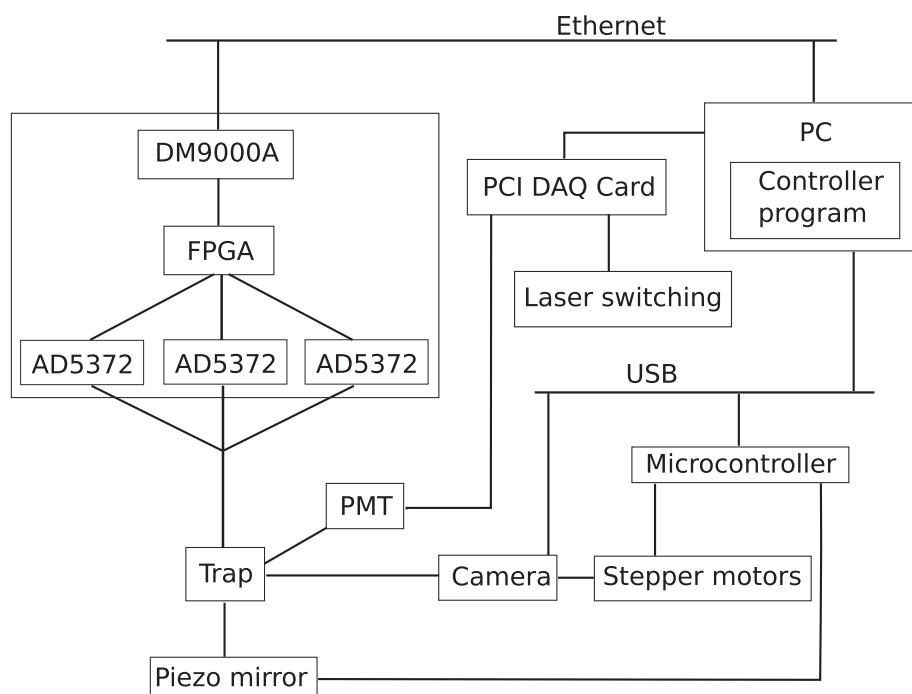


FIG. 5. Block diagram of the electrical setup of the experiment control hardware. The PC controls the trap electrodes via the FPGA system. The PC also sends data to a microcontroller which is responsible for moving the lasers and camera to follow the ion. Camera data is sent to the computer via USB and PMT counts are recorded by a PCI DAQ card. This card is also used to control the lasers.

(FPGA).⁷² A block diagram of the system is shown in Figure 5. Electrode control solutions for shuttling ions about the chip are supplied by the manufacturer and are typically calibrated for a calcium ion with voltages in the range of ± 10 V. A control program running on the host PC parses the files and applies a chip and ion-species specific mapping to determine the voltages and corresponding DAC channels. The full sequence of bytes required to control the DACs is then calculated and transmitted via UDP⁷³ over an ethernet connection to the DAC system. The FPGA reads the data via a DM9000A ethernet interface and saves it to SRAM. Upon receipt of a control signal, the FPGA will then write the data in sequence to the three DACs.

This system has proven quite capable, allowing us to control 96 electrodes over a 20 V range (± 10 V) to within 0.3 mV at an update rate of 2.4 μ s per channel with the ability to synchronize channel updates. Though rated for a 2.2 nF load, internal DAC output amplifiers are sufficient to drive the in-vacuum electronics at these speeds. The final update rate depends on the number of channels that need to be updated per step; this is typically around 5–10. The system is also low cost (around \$500) and compact. Source code (python control program and Verilog FPGA code) and schematics are available to other researchers on request.

The application of radio frequency (RF) to the trap is conventional. We use a copper can helical resonator to filter and impedance match from a power amplifier to the RF rails of the trap. The internal RF wires are shielded and take the shortest route possible from the feed-through to the trap. The design of helical resonators for this purpose has been explored by Siverns *et al.*⁷⁴ When subject to capacitive load of the trap (30 pF) our resonator operates at 24.9 MHz with a quality factor of around 200. Under typical operating conditions the RF voltage is estimated around 100 V given an RF power around 120 mW.

V. TRAP PERFORMANCE

We have demonstrated trapping of single ions in our system with a ‘Y’ trap manufactured by Sandia National Labs.³⁰ A SEM image of the surface of this trap is shown in Figure 7.

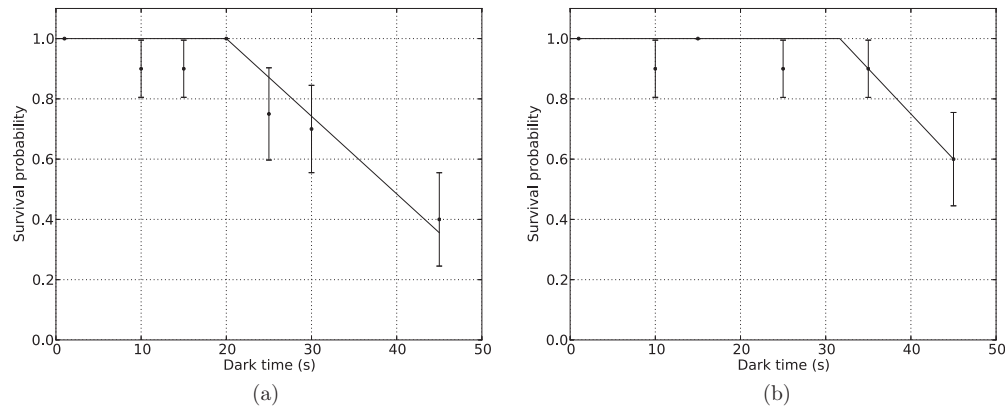


FIG. 6. Ion dark lifetime as measured following interrupting of the laser cooling. The fit to the data takes the form of Equation (1). Dark lifetimes are 20 ± 4.9 s and 31.6 ± 3.4 s for the loading region and mid-arm location respectively. (a) In the loading region and (b) In the middle of a trap arm.

Ion dark lifetimes were measured. This was done by repeatedly mechanically shuttering the re-pump laser (ensures absolute isolation) for a varying length of time and finding the probability p_l of ion loss after cooling was re-established. Because of the very long $D_{3/2}$ state lifetime (81.5 s)⁷⁵ the cooling cycle is entirely shut off without the re-pump laser.

Dark lifetimes have not been defined in a consistent way in the literature. In practice we are mostly interested in a measurement of the delay time over which all loss mechanisms are insignificant. Therefore we define the dark lifetime τ_d by making a weighted fit of

$$f(t) = \begin{cases} t < \tau_d, & 1 \\ t \geq \tau_d, & 1 - a(p_l - \tau_d) \end{cases} \quad (1)$$

as shown in Figures 6(a) and 6(b). Uncertainties for each point are $\sqrt{p_l(1 - p_l)/N}$, found assuming a binomial distribution where N is the number of measurements and the final parameter uncertainties are found from the covariance matrix produced after fitting with the Levenburg-Marquardt algorithm.

A dark lifetime of 20 ± 4.9 s was measured with the ion directly over the loading region. After shuttling the ion to the mid point of one of the trap arms an improved dark lifetime of 31.6 ± 3.4 s was measured. Some authors prefer the lifetime corresponding to 50% ion loss, which in our approximation is simply $\frac{1}{2a} + \tau_d$. Our corresponding lifetime values in this formulation are more uncertain, 39 ± 22 s and 48 ± 27 s respectively.

The secular frequencies of the trap were measured by the resonant excitation technique.⁷⁶ These were found to be 0.75 MHz, 1.5 MHz and 2.1 MHz. Given these we were able to determine a RF voltage of 96 V. This was done using boundary element model (BEM) solutions⁷⁷ of the surface potentials of this trap⁷⁸ which were scaled given the known electrode voltages. These were combined with the RF pseudo-potential calculated for a range of realistic RF voltages (50–150 V at 1 V increments) to form a set of secular potential solutions. For each of these solutions the secular frequencies were solved numerically and the best match to the three measured frequencies found.

Given the secular potential solution we were able to find the corresponding trap depth. This was done by slicing the potential through the weak axis at the trapping location and subtracting the potential at the center from the asymptote reached at large distance. We find a trap depth of 44 meV. Note that this technique does not take into account the strong stray fields above the loading region or any additional stray surface fields which are typical of these aluminum surface traps. Consequently it is most useful as a representative figure and point of comparison between chips of similar design.

We have repeated the calculation of the well depth at regions outside of the loading region and find comparable depths; around 48 meV. Therefore, we expect the observed significant difference in lifetime between locations is due to excess stray fields in the loading region rather than the different trap geometry.

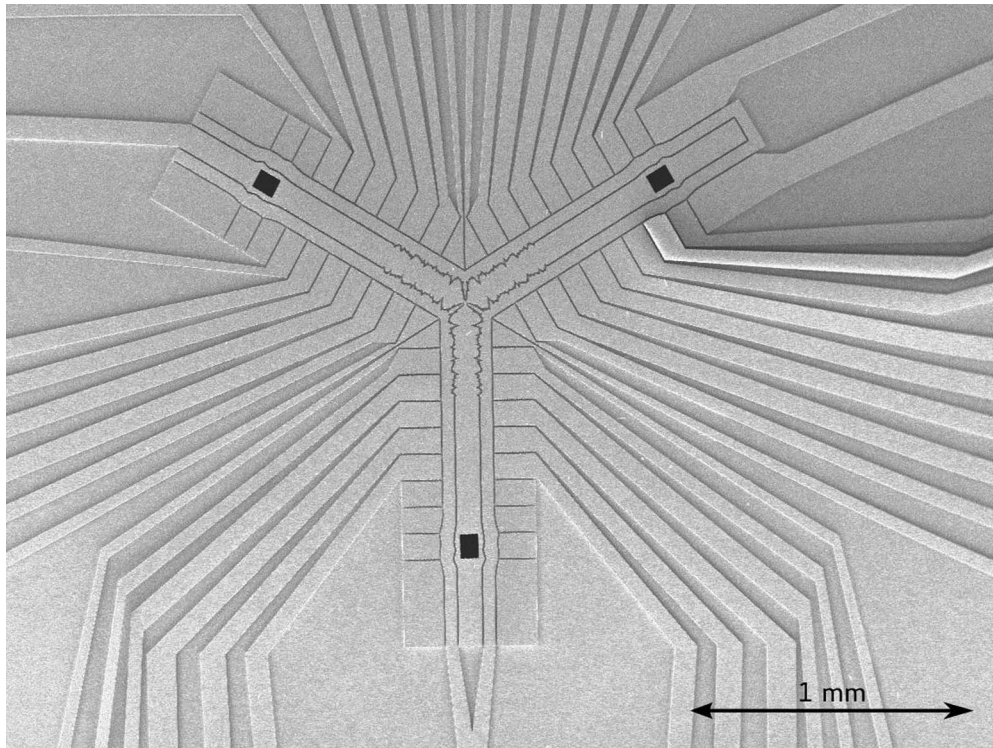


FIG. 7. SEM image of the ‘Y’ trap surface. The black rectangular sections are the loading holes. Image courtesy of Sandia National Labs.

VI. CONCLUSION

We have operated two ion trap systems based on an in vacuum soldered printed circuit board for over two years. We have not found any fundamental reliability problems and find that ion traps conforming to a 100-pin standard package can be swapped out and modifications made in a few hours; a process which has been done at least 10 times. Despite the use of materials not known for ultra-high-vacuum compatibility, stable operating pressures of around 10^{-11} Torr are readily achieved.

We have developed a custom 96-channel DC electrode control solution based on a field programmable gate array and AD5372 digital to analog converters. This solution takes advantage of the in-vacuum circuit board for mounting the output filters very close to the chip trap in order to minimize RF pickup.

The loading of barium ions in a microfabricated planar ion trap presents some challenges such as the formation of large clusters of neutral barium and surface charging from UV ionization lasers. We have developed a technique for loading and trapping barium ions and have presented results characterizing a ‘Y’ junction microfabricated planar ion trap. In this trap we have achieved good trap lifetimes of $31.6 \text{ s} \pm 3.4 \text{ s}$.

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SEM images (Figures 4 and 7) courtesy of Sandia National Laboratories, New Mexico, USA.

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